**M.E. (VLSI DESIGN)**  
*Curriculum for the Academic Year 2007-2008*  
*(Minimum credits to be earned: 88)*

<table>
<thead>
<tr>
<th>Code No.</th>
<th>Course</th>
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<td><strong>SEMESTER 1: THEORY</strong></td>
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<td>07VL01*</td>
<td>Applied Mathematics for Electronics Engineers</td>
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List of Electives

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<td>07VL21</td>
<td>CMOS VLSI Design</td>
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<td>07VL22#</td>
<td>Analog VLSI Design</td>
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<td>07VL23</td>
<td>Testing of VLSI Circuits</td>
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<td>Low Power VLSI Design</td>
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<td>07VL25</td>
<td>Design of Semiconductor Memories</td>
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<td>07VL26</td>
<td>VLSI Technology</td>
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<td>Embedded Systems</td>
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<td>Physical Design of VLSI Circuits</td>
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<td>VLSI Signal Processing</td>
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<td>Genetic Algorithms and their Applications</td>
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<td>Advanced Microprocessors and Microcontrollers</td>
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<td>Reliability Engineering</td>
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<td>Electromagnetic Interference and Compatibility in System Design</td>
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<td>Speech and Audio Signal Processing</td>
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<td>DSP Processor Architecture and programming</td>
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<td>Neural Networks, Architectures and Applications</td>
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* Common with M.E.-AE & CO
# Common with M.E.-AE
† Common with M.E.- CO

07VL01/ 07AE01/ 07CO01  **Applied Mathematics for Electronics Engineers**  4 0 0 4

**Unit I**
Linear Algebraic Equation and Eigen Value Problems

10 Hours

**Unit II**
Wave Equation
Solution of initial and boundary value problems- Characteristics- D’Alembert’s Solution - Significance of characteristic curves - Laplace transform solutions for displacement in a long string - a long string under its weight - a bar with prescribed force on one end- free vibrations of a string.

10 Hours

**Unit III**
Special Functions

Bessel’s equation - Bessel Functions- Legendre’s equation - Legendar polynomials -Rodrigue’s formula - Recurrence relations- generating functions and orthogonal property for Bessel functions - Legendre polynomials.  

10 Hours

Unit IV

Random Variables

One dimensional Random Variable - Moments and MGF – Binomial, Poisson, Geometrical, Normal Distributions- Two dimensional Random Variables – Marginal and Conditional Distributions – Covariance and Correlation Coefficient - Functions of Two dimensional random variable.  

10 Hours

Unit V

Queueing Theory

Single and Multiple server Markovian queueing models - Steady state system size probabilities – Little’s formula - Priority queues - M/G/1 queueing system – P.K. formula.  

10 Hours

Text Books


References


07VL02/ 07AE33 Digital Signal Processing Integrated Circuits

4 0 0 4

Unit I

DSP Integrated Circuits and VLSI circuit Technologies

Standard digital signal processors-Application specific IC’s for DSP - DSP systems - DSP system design - Integrated circuit design - MOS transistors - MOS logic - VLSI process technologies - Trends in CMOS technologies.  

10 Hours

Unit II
Digital Signal Processing

Unit III
Digital Filters and Finite Word Length Effects

Unit IV
DSP Architectures and Synthesis of DSP Architectures
DSP system architectures - Standard DSP architecture - Ideal DSP architectures - Multiprocessors and multicomputers - Systolic and Wave front arrays - Shared memory architectures - Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bit-serial PEs.

Unit V
Arithmetic Units and Integrated Circuit Design
Conventional number system - Redundant Number system - Residue Number System - Bit-parallel and Bit-Serial arithmetic - Basic shift accumulator - Reducing the memory size - Complex multipliers - Improved shift – accumulator - Layout of VLSI circuits - FFT processor - DCT processor and Interpolator as case studies.

Text Books

References
Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State
Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart
–ASMRealization.

10 Hours

Unit II
Asynchronous Sequential Circuit Design
Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC –
State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic
Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller –
Mixed Operating Mode Asynchronous Circuits.

10 Hours

Unit III
Fault Diagnosis and Testability Algorithms
Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi
Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA’s – Fault in PLA –

10 Hours

Unit IV
Synchronous Design Using Programmable Devices
EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a
Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD

10 Hours

Unit V
System Design Using VHDL
VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and
Simulation of VHDL Code – Modeling using VHDL – Flip Flops – Registers – Counters –
Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary

10 Hours

Text books

References

07VL04/ 07AE04/ 07CO42 VLSI Design Techniques
Unit I
MOS Transistor Theory and Process Technology
NMOS and PMOS transistors - Threshold voltage - Body effect - Design equations - Second order effects - MOS models and small signal AC characteristics - Basic CMOS technology.  

10 Hours

Unit II
Inverters and Logic Gates
NMOS and CMOS Inverters - Stick diagram - Inverter ratio - DC and transient characteristics - Switching times - Super buffers - Driving large capacitance loads - CMOS logic structures - Transmission gates - Static CMOS design - Dynamic CMOS design.

10 Hours

Unit III
Circuit Characterization and Performance Estimation
Resistance estimation - Capacitance estimation - Inductance - Switching characteristics - Transistor sizing - Power dissipation and design margining - Charge sharing - Scaling.

10 Hours

Unit IV
VLSI System Components Circuits and System Level Physical Design
Multiplexers - Decoders - Comparators - Priority encoders - Shift registers - Arithmetic circuits - Ripple carry adders - Carry look ahead adders - High-speed adders – Multipliers - Physical design - Delay modeling - Cross talk - Floor planning - Power distribution - Clock distribution - Basics of CMOS testing.

10 Hours

Unit V
VERILOG Hardware Description Language

10 Hours

Text Books

References
Unit I

Principles of Parallel Processing
Multiprocessors and Multicomputers - Multivector and SIMD Computers - PRAM and VLSI Models - Conditions of Parallelism - Program Partitioning and scheduling - Program flow mechanisms - Parallel processing applications - Speed up performance law.  

Unit II

Processor and Memory Organization
Advanced processor technology - Superscalar and vector processors - Memory hierarchy technology - Virtual memory technology - Cache memory organization - Shared memory organization.  

Unit III

Pipeline and Parallel Architecture
Linear pipeline processors - Non linear pipeline processors - Instruction pipeline design - Arithmetic design - Superscalar and super pipeline design - Multiprocessor system interconnects - Message passing mechanisms.  

Unit IV

Vector, Multithread and Dataflow Architecture
Vector processing principle - Multifactor Multiprocessors - Compound Vector processing - Principles of multithreading - Fine grain multicomputers - Scalable and multithread architectures - Dataflow and hybrid architectures.  

Unit V

Software and Parallel Processing
Parallel programming models - Parallel languages and compilers - Parallel programming environments - Synchronization and Multiprocessing modes - Message passing program development - Mapping programs onto Multicomputers - Multiprocessor UNIX design goals - MACH/OS kernel architecture - OSF/1 architecture and applications.  

Text Book


References


Total: 50 Hours
Unit I
Basic Semiconductor Physics

10 Hours

Unit II
Bipolar Device Modeling
Injection and Transport Model - Continuity Equation - Diode Small Signal and Large Signal (Change Control Model) - Transistor Models: Ebber - Molls and Gummel Port Model - Mextram model - SPICE modeling temperature and area effects.

10 Hours

Unit III
MOSFET Modeling
Introduction - Inversion Layer - MOS Transistor Current - Threshold Voltage - Temperature Short Channel and Narrow Width Effect - Models for Enhancement - Depletion Type MOSFET - CMOS Models in SPICE.

10 Hours

Unit IV
Parameter Measurement

10 Hours

Unit V
Optoelectronic Device Modeling
Static and Dynamic Models - Rate Equations - Numerical Technique - Equivalent Circuits - Modeling of LEDs - Laser Diode and Photo detectors.

10 Hours

Total: 50 Hours

Text Books


References


1. Modeling of Sequential Digital system using VHDL.
3. Design and Implementation of ALU using FPGA.
4. Simulation of NMOS and CMOS circuits using SPICE.
5. Modeling of MOSFET using C.
8. Implementation of MAC Unit using FPGA.

07VL12 VLSI Design Laboratory II

1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 Bit Sliced processor in FPGA / CPLD.
5. Implementation of model train controller using embedded microcontroller.
6. System design using PLL.

07VL07/ 07AE07 Analysis and Design of Analog Integrated Circuits

Unit I
Models for Integrated Circuit Active Devices
Depletion region of a PN junction – Large signal behavior of bipolar transistor- Small signal model of bipolar transistor- Large signal behavior of MOSFET- Small signal model of MOS transistor- Short channel effects in MOS transistors – Weak inversion in MOS transistors- Substrate current flow in MOS transistors. 10 Hours

Unit II
Circuit Configuration for Linear IC
Current Sources - Analysis of Difference Amplifiers with Active Load Using BJT and FET - Supply and Temperature Independent Biasing Techniques - Voltage References. Output Stages: Emitter Follower - Source Follower and Push Pull Output Stages. 10 Hours

Unit III
Operational Amplifiers
Analysis of operational amplifiers circuit - Slew rate model and high frequency analysis - Frequency response of integrated circuits - Single stage and multistage amplifiers - Operational amplifier noise

Unit IV
Analog Multiplier and PLL
Analysis of four quadrant and variable transconductance multiplier - voltage controlled oscillator - Closed loop analysis of PLL - Monolithic PLL design in integrated circuits - Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature 10 Hours
Unit V

Analog Design with MOS Technology
MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

10 Hours

Text Books


References


Total: 50 Hours
High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.  
10 Hours

**Text Books**


**References**


07VL09/ 07AE34 ASIC Design

Unit I
Introduction to ASICS, CMOS Logic and ASIC Library Design
Types of ASICs - Design flow - CMOS transistors - CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.  
10 Hours

Unit II
Programmable ASICS, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.  
10 Hours

Unit III
Programmable ASIC Interconnect, Programmable ASIC Design Software And Low Level Design Entry
10 Hours

Unit IV
Logic Synthesis, Simulation And Testing
Verilog and logic synthesis - VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.  
10 Hours

Unit V
ASIC Construction, Floor Planning, Placement And Routing
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

10Hours

Total: 50 Hours

Text Books


References


07VL13 Advanced VLSI Design Laboratory

1. Layout design and simulation of static digital circuits.
2. Layout design and simulation of dynamic digital circuits.
3. Design and simulation of LFSR.
5. IC layout design for Analog circuits.
6. IC layout design for digital circuits.
7. Group projects on design, analysis, and layout for digital circuits.

ELECTIVE

07VL21 CMOS VLSI Design

Unit I
MOS Transistor Theory

Unit II
CMOS Processing Technology.
Silicon semiconductor technology. Wafer processing, Oxidation, epitaxy, deposition, Ion implantation. CMOS technology. N-well, p-well process. Silicon on insulator. CMOS process enhancement. Interconnect and circuit elements. Layout design rules. Latchup. 10 Hours

Unit III
Circuit Characteristics And Performance Estimation

Unit IV
CMOS Circuit And Logic Design

Unit V
CMOS Subsystem Design

Text Books

References

07VL22/ 07AE30 Analog VLSI Design

Unit I
Basic CMOS Circuit Techniques, Continuous Time and Low-Voltage Signal Processing

Unit II
Basic BICMOS Circuit Techniques, Current -Mode Signal Processing and Neural Information Processing
Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating -
Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina. 10 Hours

Unit III
Sampled-Data Analog Filters, Over Sampled A/D Converters and Analog Integrated Sensors

Unit IV
Design for Testability and Analog VLSI Interconnects

Unit V
Statistical Modeling And Simulation, Analog Computer-Aided Design and Analog and Mixed Analog-Digital Layout

Total: 50 Hours

Text Books

References

07VL23 Testing of VLSI Circuits 4 0 0 4

Unit I
Fault Simulation
Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation. 10 Hours

Unit II
Test Generation
Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits. **10 Hours**

**Unit III**  
**Testable Design**  
Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches. **10 Hours**

**Unit IV**  
**Built In Self Test**  
Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs **10 Hours**

**Unit V**  
**Fault Diagnosis**  
Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis. **10 Hours**

**Text Books**

**References**

**07VL24/ 07AE31 Low Power VLSI Design**  
**4 0 0 4**

**Unit I**  
**Power Dissipation in CMOS**  
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design. **10 Hours**

**Unit II**  
**Power Optimization**  
Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers. **10 Hours**

**Unit III**  
**Design of Low Power CMOS Circuits**  
Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques **10 Hours**

**Unit IV**  
**Power Estimation**
Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis.

Unit V
Synthesis and Software Design for Low Power
Synthesis for low power –Behavioral level transforms- Software design for low power

Text Books

References

07VL25 Design of Semiconductor Memories

Unit I
Random Access Memory Technologies Static random access memories (srams)
SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.
Dynamic random access memories (drams):

Unit II
Nonvolatile memories
Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-AdvancedFlash Memory Architecture.

Unit III
Memory fault modeling, testing, and memory design for Testability and fault tolerance
Unit IV
Semiconductor Memory Reliability and Radiation Effects

Unit V
Packaging Technologies
Total:  50 Hours

Text Books

References

07VL26 VLSI Technology 4 0 0 4

Unit I
Crystal Growth, Wafer Preparation, Epitaxy and Oxidation
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects. 10 Hours

Unit II
Lithography and Reactive Plasma Etching
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, reactive Plasma Etching techniques and Equipments,  

10 Hours

Unit III
Deposition, Diffusion, Ion Implantation and Metalisation

10 Hours

Unit IV
Process Simulation and VLSI Process Integration

10 Hours

Unit V
Analytical, Assembly Techniques and Packaging of VLSI Devices.

10 Hours

Total: 50 Hours

Text Books

References

07VL27/ 07AE26/ 07CO39 Embedded Systems

4 0 0 4

Unit I
Embedded Architecture
Embedded systems Overview, Design Challenge – Optimizing design metrics, Processor Technology, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioral Description, Design Example: Model Train Controller.  

10 Hours

Unit II
Embedded Processor and Computing Platform
Unit I
Introduction to VLSI Technology
Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of
gates, field programmable gate array (FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms

10 Hours

Unit II
Placement Using Top-Down Approach

10 Hours

Unit III
Routing Using Top Down Approach:

10 Hours

Unit IV
Performance Issues In Circuit Layout:

10 Hours

Unit V
Single Layer Routing, Cell Generation and Compaction

10 Hours

Total: 50 Hours

Text Books


References


07VL29/ 07AE32 VLSI Signal Processing 4 0 0 4

Unit I
Introduction to DSP
Introduction To DSP Systems -Typical DSP algorithms Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power. 10 Hours

Unit II
Retiming
Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd-Even Merge-Sort architecture, parallel rank-order filters. 10 Hours

Unit III
Fast Convolution
Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter. 10 Hours

Unit IV
Bit-Level Arithmetic Architectures
Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh- Wooley carry-save multiplication tabular form and implementation, design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement. 10 Hours

Unit V
Programming Digital Signal Processors
Numerical Strength Reduction – sub expression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining-synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design. 10 Hours
Text Books


References


07VL30/ 07AE36 Genetic Algorithms and their Applications 4 0 0 4

Unit I
Overview of Genetic Algorithm
Introduction, GA Techniques-Steady State Algorithm-Fitness, Scaling-Inversion 10 Hours

Unit II
Genetic Algorithm for VLSI Design

Unit III
Advanced Algorithms in Genetic Algorithm
Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Gas - Standard cell placement-GASP algorithm-unified algorithm. 10 Hours

Unit IV
Genetic Algorithm for VLSI Testing
Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures. 10 Hours

Unit V
Applications
Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding-fitness function-GA vs. Conventional Algorithm. 10 Hours

Total: 50 Hours

Text Books

References

1. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley
   Maria Bernard Vellasco “Evolution Electronics: Automatic Design of electronic
   Programming Automatic programming and Automatic Circuit Synthesis”, 1st

07VL31/ 07AE05/ 07CO41 Advanced Microprocessors and Microcontrollers

Unit I
Microprocessor Architecture
Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy –
register file – Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction
pipeline – pipeline hazards – Instruction level parallelism – reduced instruction set – Computer
principles – RISC versus CISC – RISC properties – RISC evaluation – On-chip register files
versus cache evaluation

10 Hours

Unit II
High Performance CISC Architecture – Pentium
The software model – functional description – CPU pin descriptions – RISC concepts – bus
operations – Super scalar architecture – pipe lining – Branch prediction – The instruction and
caches – Floating point unit –protected mode operation – Segmentation – paging – Protection –
 multitasking – Exception and interrupts – Input /Output – Virtual 8086 model – Interrupt
processing -Instruction types – Addressing modes – Processor flags – Instruction set -
programming the Pentium processor.

10 Hours

Unit III
High Performance RISC Architecture: ARM
The ARM architecture – ARM assembly language program – ARM organization and
implementation – The ARM instruction set - The thumb instruction set – ARM CPU cores.

10 Hours

Unit IV
Motorola 68HC11 Microcontrollers
Instructions and addressing modes – operating modes – Hardware reset – Interrupt system –
Parallel I/O ports – Flags – Real time clock – Programmable timer – pulse accumulator – serial
communication interface – A/D converter – hardware expansion – Assembly language
Programming.

10 Hours

Unit V
PIC Micro Controller
CPU architecture – Instruction set - Interrupts – Timers – I/O port expansion –I2C bus for
peripheral chip access – A/D converter – UART

10 Hours

Total: 50 Hours

References
07VL32/ 07AE40 Reliability Engineering

Unit I
Probability Plotting and Load-Strength Interference
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference, Safety margin and loading roughness on reliability. 10 Hours

Unit II
Reliability Prediction, Modelling and Design
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis. 10 Hours

Unit III
Electronics and Software Systems Reliability
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces. 10 Hours

Unit IV
Reliability Testing and Analysis
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring. 10 Hours

Unit V
Manufacture and Reliability Management
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability. 10 Hours

Total: 50 Hours

Text Books
1. Patrick D.T. O'Connor, David Newton and Richard Bromley, “Practical Reliability
References


Unit I
EMI Environment
EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.
10 Hours

Unit II
EMI Coupling Principles
Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.
10 Hours

Unit III
EMI/EMC Standards and Measurements
Civilian standards - FCC,CISPR,IEC,EN,Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures 462. 10 Hours

Unit IV
EMI Control Techniques
Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting. 10 Hours

Unit V
EMC Design of PCBs
PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models. 10 Hours

Total: 50 Hours

Text Books

References


07VL34/ 07CO26 Speech and Audio Signal Processing

Unit I
Mechanics of Speech

10 Hours

Unit II
Time Domain Methods for Speech Processing

10 Hours

Unit III
Frequency Domain Method for Speech Processing

10 Hours

Unit IV

10 Hours

Unit V
Application of Speech & Audio Signal Processing

10 Hours

Total: 50 Hours

Text Books

References


07VL35/ 07CO24 DSP Processor Architecture and programming

Unit I
Fundamentals of Programmable DSPs
Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P- DSPs - Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

10 Hours

Unit II
TMS320C5X Processor
Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

10 Hours

Unit III
TMS320C3X processor
Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design.

10 Hours

Unit IV
ADSP Processors
Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

10 Hours

Unit V
Advanced Processors

10 Hours

Total: 50 Hours

Text Book

New Delhi, 2003.

References


07VL36/ 07AE21 Neural Networks, Architectures and Applications

Unit I
Back Propagation

10 Hours

Unit II
Statistical Methods

10 Hours

Unit III
Counter Propagation Network and Self Organizing Maps
CPN building blocks - CPN data processing. SOM data processing - Applications.  

10 Hours

Unit IV
Adaptive Resonance Theory and Spatio Temporal Pattern Classification
ART network description - ART1-ART2 - Application. The formal avalanche - Architecture of spatio temporal networks - The sequential competitive avalanche field - Applications of STNs.  

10 Hours

Unit V
Neo – Congnitron
Cognitron - Structure & training - The neocognitron architecture - Data processing - Performance - Addition of lateral inhibition and feedback to the neocognitron. Optical neural networks - Holographic correlators.  

10 Hours

Total: 50 Hours

Text Books


References