M.E. (VLSI Design)

2026 Regulations - Curriculum & Syllabi

Stay Ahead

BANNARI AMMAN INSTITUTE OF TECHNOLOGY

An Autonomous Institution Affiliated to Anna University – Chennai • Approved by AICTE • Accredited by NAAC with "A+" Grade

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CONTENTS **Page No.**

VISION OF THE DEPARTMENT

To be a centre of excellence in VLSI Design education and research by developing competent professionals, fostering innovation in semiconductor technologies, and contributing to sustainable societal and industrial advancement.

MISSION OF THE DEPARTMENT

M1: Develop strong knowledge and practical skills in semiconductor devices, IC design, FPGA, physical design, verification, and emerging VLSI technologies.

M2: Promote research, innovation, entrepreneurship, and industry collaboration in semiconductor and VLSI domains by engaging students in advanced design projects, product development, and interdisciplinary research activities.

M3: Develop graduates with professional competence, leadership qualities, lifelong learning ability, ethical values, and social responsibility to contribute effectively to the semiconductor industry, academia, and society.

PROGRAM OUTCOMES (POs)

PO	Graduate Attribute	Programme Outcome
1	Research aptitude	An ability to independently carry out research/investigation and development work to solve practical problems.
2	Technical documentation	An ability to write and present a substantial technical report/document.
3	Technical competence	Students should be able to demonstrate a degree of mastery over VLSI Design and Analysis.
4	Engineering Design	An ability to apply advanced concepts of VLSI for chip design with state of art tools.
5	The engineer and society	An ability to evolve customizable Chip Design for different Engineering applications.
6	Environment and sustainability	An ability to provide paradigm solution in the development of customized prototypes and chip design which have social and global relevance.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

I. Apply advanced knowledge of semiconductor devices, VLSI design methodologies, and electronic design automation tools to develop innovative integrated circuit and system solutions.

II. Pursue successful careers in semiconductor industries, research organizations, entrepreneurship, and higher education through continuous learning and professional development.

III. Demonstrate leadership, ethical responsibility, teamwork, and effective communication skills while addressing technological and societal challenges through sustainable engineering practices.

M.E VLSI Design - R2026 Minimum Credits to be Earned: 73										
I SEMESTER										
Course Code	**Course Title**	**L**	**T**	**P**	**C**	**Hours / Week**	**Maximum Marks**			**Category**
							CA	**SEE**	**CA**	
26VL11	Research Methodology and IPR	2	0	0	2	2	40	60	100	ES
26VL12	Graph Theory and Optimization Techniques	3	0	0	3	3	40	60	100	BS
26VL13	Digital Design with FPGA	3	0	0	3	3	40	60	100	PC
26VL14	Digital Integrated Circuit Design	3	0	0	3	3	40	60	100	PC
26VL15	Semiconductor Device Modelling	3	0	0	3	3	40	60	100	PC
26VL16	Analog Integrated Circuit Design	3	0	0	3	3	40	60	100	PC
26VL17	Digital Design with FPGA Laboratory	0	0	4	2	3	60	40	100	PC
26VL18	Digital and Analog Integrated Circuit Design Laboratory	0	0	4	2	3	60	40	100	PC
-	Industry Oriented Course*	1	0	0	1	1	100	0	100	SD
	Audit course I*	2	0	0	-	2	100	0	100	EEC
Total		**20**	**0**	**8**	**22**	**26**	**-**	**-**	**-**	**-**
II SEMESTER										
Course Code	**Course Title**	**L**	**T**	**P**	**C**	**Hours / Week**	**Maximum Marks**			**Category**
							CA	**SEE**	**CA**	
26VL21	VLSI Scripting Languages	3	0	0	3	3	40	60	100	PC
26VL22	System Verilog for Verification	3	0	0	3	3	40	60	100	PC
26VL23	VLSI Physical Design	3	0	0	3	3	40	60	100	PC
26VL24	Design for Testability (DFT)	3	0	0	3	3	40	60	100	PC
	Program Elective I	3	0	0	3	3	40	60	100	PE
	Program Elective II	3	0	0	3	3	40	60	100	PE
26VL27	RTL to GDSII Laboratory	0	0	4	2	4	60	40	100	PC
26VL28	Design Verification Laboratory	0	0	4	2	4	60	40	100	PC
26VL29	Mini Project	0	0	4	2	4	100	0	100	PC
	Audit course II*	2	0	0	-	2	100	0	100	EEC
Total		**20**	**0**	**12**	**24**	**32**	**-**	**-**	**-**	**-**

III SEMESTER										
Course Code	**Course Title**	**L**	**T**	**P**	**C**	**Hours / Week**	**Maximum Marks**			**Category**
							CA	**SEE**	**CA**	
	Program Elective III	3	0	0	3	3	40	60	100	PE
	Program Elective IV	3	0	0	3	3	40	60	100	PE
	Program Elective V	3	0	0	3	3	40	60	100	PE
26VL34	Dissertation Phase I	0	0	12	6	12	60	40	100	EEC
Total		**9**	**0**	**12**	**15**	**21**	**-**	**-**	**-**	**-**

IV SEMESTER										
Course Code	**Course Title**	**L**	**T**	**P**	**C**	**Hours / Week**	**Maximum Marks**			**Category**
							CA	**SEE**	**CA**	
26VL41	Dissertation Phase II	0	0	24	12	24	60	40	100	EEC
Total		**0**	**0**	**24**	**12**	**24**	**-**	**-**	**-**	**-**

BS - Basic Sciences
ES - Engineering Sciences
HSS - Humanities and Social Sciences
PC - Professional Core
PE - Professional Elective
EEC - Employability Enhancement Course
CA - Continuous Assessment
ES - End Semester Examination
SD - Skill Development

LIST OF PROFESSIONAL ELECTIVES										
Course Code	**Course Title**	**L**	**T**	**P**	**C**	**Hours / Week**	**Maximum Marks**			**Category**
							CA	**SEE**	**Total**	
26VL51	VHDL Programming	3	0	0	3	3	40	60	100	PE
26VL52	Genetic Algorithms and their Applications	3	0	0	3	3	40	60	100	PE
26VL53	Embedded Systems Design	3	0	0	3	3	40	60	100	PE
26VL54	Digital Signal Processing IC Design	3	0	0	3	3	40	60	100	PE
26VL55	Advanced Computer Architecture	3	0	0	3	3	40	60	100	PE
26VL56	RISC-V Processor Design	3	0	0	3	3	40	60	100	PE
26VL57	System-on-Chip Design	3	0	0	3	3	40	60	100	PE
26VL58	FPGA-based SoC Design	3	0	0	3	3	40	60	100	PE
26VL59	Network-on-Chip (NoC) Design	3	0	0	3	3	40	60	100	PE
26VL60	VLSI Technology	3	0	0	3	3	40	60	100	PE
26VL61	ASIC Design Methodology	3	0	0	3	3	40	60	100	PE
26VL62	Low Power VLSI Design	3	0	0	3	3	40	60	100	PE
26VL63	Static Timing Analysis	3	0	0	3	3	40	60	100	PE
26VL64	Semiconductor Memory Design	3	0	0	3	3	40	60	100	PE
26VL65	VLSI Signal Processing	3	0	0	3	3	40	60	100	PE
26VL66	Mixed-Signal IC Design	3	0	0	3	3	40	60	100	PE
26VL67	Analog Layout Design	3	0	0	3	3	40	60	100	PE
26VL68	RF Integrated Circuit Design	3	0	0	3	3	40	60	100	PE
26VL69	Design Verification Methodologies - UVM)	3	0	0	3	3	40	60	100	PE
26VL70	Hardware Security for VLSI Systems	3	0	0	3	3	40	60	100	PE
26VL71	Cryptography & Network Security	3	0	0	3	3	40	60	100	PE
26VL72	Chip Packaging & Heterogeneous Integration	3	0	0	3	3	40	60	100	PE
26VL73	AI Hardware Accelerators	3	0	0	3	3	40	60	100	PE
26VL74	Hardware Acceleration for Machine Learning	3	0	0	3	3	40	60	100	PE
26VL75	Neuromorphic Computing	3	0	0	3	3	40	60	100	PE
26VL76	Nanoelectronics	3	0	0	3	3	40	60	100	PE
26VL77	Quantum Circuits	3	0	0	3	3	40	60	100	PE

LIST OF AUDIT COURSES I & II										
26XE01	English for Research Paper Writing	2	0	0	-	2	100	0	100	EEC
26XE02	Cost Management of Engineering Projects	2	0	0	-	2	100	0	100	EEC
26XE03	Stress Management	2	0	0	-	2	100	0	100	EEC
26XE04	Disaster Management	2	0	0	-	2	100	0	100	EEC
26XE05	Value Education	2	0	0	-	2	100	0	100	EEC

26VL11	RESEARCH METHODOLOGY AND IPR	L	T	P	C
		2	0	0	2

Prerequisite	Assessment Pattern		
• Knowledge of research process	CIA	SEE	Total
• Research ethics	40	60	100

Course Objectives:

- Understand the techniques for research problem formulation, analysis and solution.
- Analyze literature surveys and prepare reports based on research ethics.
- Develop research proposals and apply assessment procedures to review.
- Develop patents using the IPR & PCT guidelines.
- Adapt the licensing process for patents and analyse the developments of IPR

Course Outcomes (COs)

At the end of the course, students will be able to

1. Formulate the research problems and identify the approaches to solve the problems
2. Analyze literature surveys and prepare reports based on research ethics.
3. Develop research proposals and apply assessment procedures to review.
4. Develop patents using the IPR & PCT guidelines.
5. Adapt the licensing process for patents and analyse the developments of IPR

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	3	2	2	3	2	3
CO 2	3				1	3
CO 3	3			1	1	2
CO 4	3				1	1
CO 5	3			1	1	1

Unit I INTRODUCTION TO RESEARCH PROBLEM 6 Hours

Meaning of research problem - Sources of research problem - Criteria characteristics of a good research problem- errors in selecting a research problem-scope and objectives of research problem-Approaches of Investigations of solutions for research problem-Data collection-Analysis-Interpretation-Necessary instrumentations.

Unit II LITERATURE REVIEW 6 Hours

Effective Literature studies approaches-analysis-Plagiarism-Research ethics- Review of the literature, Searching the existing literature, reviewing the selected literature, developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed.

Unit III TECHNICAL WRITING/PRESENTATION 6 Hours

Effective technical writing-how to write report-paper-Developing a research proposal-Format of Research proposal-a presentation and assessment by a review committee.

Unit IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS(IPR) 6 Hours

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: Technological research, Innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grant Patents, Patenting under Patent Cooperation Treaty(PCT).

Unit V INTELLECTUAL PROPERTY RIGHT(IPR) 6 Hours

Patent Rights: Scope of Patent Rights, Licensing and transfer of Technology, Patent information and Databases-Geographical Indications. New Developments in IPR: Administration of Patent system, IPR of Biological systems, Computer Software-Traditional knowledge - Case studies.	
Term Work Activity	
Quiz, Assignments, and Seminar Presentations.	
Self-Learning Activity	
NPTEL Course: https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_ge79	
Total	**30 Hours**

References:

1. Wayne Goddard and Stuart Melville, Research methodology-An Introduction, 2nd Edition, Juta and Company Ltd, 2007.
2. Halbert, Resisting Intellectual Property, Taylor & Francis Ltd, 2007
3. Robert P.Merges, Peter S.Menell, Mark.A.Lemley, Intellectual property in new technological age, 2016.
4. T.Ramappa, Intellectual Property Rights under WTO, S.Chand, 2008.
5. Ranjit Kumar, 2nd Edition, Research Methodology: A Step by Step Guide for beginners, 2010.
6. C.R.Kothari, Gaurav Garg, Research Methodology, Methods and Techniques, 4th Edition, New Age International Publishers, 2018.

26VL12	GRAPH THEORY AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	0	0	3

Prerequisite	Assessment Pattern		
• Knowledge of basic mathematics and algebra • Understanding of basic algorithms and problem-solving techniques	CIA	SEE	Total
	40	60	100

Course Objectives:

- To understand the fundamental concepts of graph theory and their applications in modeling real-world problems.
- To develop analytical skills in graph algorithms, shortest path methods, and graph traversal techniques for computational problem solving.
- To formulate and solve linear programming problems using graphical, simplex, transportation, and assignment methods.
- To apply nonlinear programming techniques including constrained optimization, KKT conditions, and quadratic programming for engineering applications.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Analyze and apply concepts of graphs, including graph models, types of graphs, matrix representation, connectivity, Euler and Hamilton paths, and spanning trees to solve real-world problems.
2. Develop and implement graph algorithms such as shortest path and depth-first search, and evaluate their performance for solving computational problems.
3. Formulate and solve linear programming problems using graphical and simplex methods, including transportation and assignment models for optimization.
4. Apply optimization techniques to solve constrained non-linear problems using Lagrangian methods, KKT conditions, and quadratic programming.
5. Analyze and apply simulation techniques, including Monte Carlo methods and queuing models, and solve project scheduling problems using CPM, PERT, and sequencing models.

Articulation Matrix

Co No	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	2		2		1	
CO 2	2				1	
CO 3	2	1		1		
CO 4	2			1	2	1
CO 5	2	1	3	1	1	2

Unit I GRAPHS 9 Hours

Graphs and graph models - Graph terminology and special types of graphs - Matrix representation of graphs and graph isomorphism - Connectivity- Euler and Hamilton paths - Trees - Spanning trees.

Unit II GRAPH ALGORITHM 9 Hours

Graph Algorithms - Directed graphs - Some basic algorithms - shortest path algorithms - Depth - First search on a graph - Theoretic algorithms - Performance of graph theoretic algorithms - Graph theoretic computer languages.

Unit III LINEAR PROGRAMMING 9 Hours

Formulation - Graphical solution - Simplex method - Two-phase method - Transportation and Assignment Models.

Unit IV	**NON LINEAR PROGRAMMING**	**9 Hours**
Constrained Problems, Equality constraints- Lagrangean Method, Inequality constraints, Karush, Kuhn-Tucker {KKT) conditions - Quadratic Programming.		
Unit V	**SIMULATION AND NETWORK MODEL**	**9 Hours**
Monte Carlo Simulation, Types of Simulation, Elements of Discrete Event Simulation, Generation of Random Numbers, Applications to Queuing systems - Project network, CPM and PERT networks, Critical path scheduling - Sequencing models.		
Term Work Activity		
Quiz, Assignments, and Seminar Presentations.		
Self-Learning Activity		
NPTEL Course: https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_ee148		
	Total	**45 Hours**

References:

1.Sharma, J. K. Operation Research (3rd ed.). Macmillan Publishers India Ltd., 2009.

2.West, D. B. Introduction to Graph Theory. Pearson Education, 2015.

3.Balakrishna, R., & Ranganathan, K. A Textbook of Graph Theory. Springer Science and Business Media, 2012.

4.Deo, N. Graph Theory with Applications to Engineering and Computer Science. Dover Publications, Inc., 2016.Rao, G. S. S. B. Discrete Structures and Graph Theory. Scitech Publications Pvt. Limited, 2015.

5.Natarajan, A. M., Balasubramani, P., & Tamilarasi, A. Operations Research. Pearson Education Pvt. Limited, 2014.

26VL13	DIGITAL DESIGN WITH FPGA	L	T	P	C
		3	0	0	3

Prerequisite	Assessment Pattern		
• Basic knowledge of Verilog HDL • Understanding of Verilog/VHDL Programming	CIA	SEE	Total
	40	60	100

Course Objectives:

- Develop an understanding of FPGA architectures, programmable logic technologies, and FPGA-based digital design methodologies.
- Develop the ability to design, synthesize, analyze, and optimize RTL-based digital systems for FPGA implementation.
- Introduce FPGA-based system implementation, processor integration, peripheral interfacing, and hardware-software co-design.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Understand the architecture, programmable resources, configuration technologies, and implementation flow of modern FPGA devices.
2. Design and synthesize RTL-based combinational, sequential, memory, and arithmetic circuits for FPGA implementation.
3. Analyze and optimize FPGA designs considering resource utilization, timing, area, and power constraints.
4. Design and implement FPGA-based digital systems and processor-based architectures, including RISC-V-based systems and peripheral interfaces.
5. Apply hardware-software co-design techniques for FPGA-based systems, including processor–FPGA integration and hardware acceleration.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	1			2		
CO 2	1	1	2			
CO 3	2	1	3		2	
CO 4	2		3	3	3	
CO 5	2	1	3	3	3	2

Unit I PROGRAMMABLE LOGIC DEVICES AND FPGA ARCHITECTURE 9 Hours

PROM, PLA, PAL and CPLD – Introduction to FPGA – FPGA versus ASIC – FPGA implementation flow – FPGA EDA tools – FPGA configuration technologies – FPGA architecture – Configurable Logic Blocks – LUT-based function generators – Flip-Flops and multiplexers – Programmable interconnections and routing – Input/Output Blocks – Block RAM – DSP blocks – Clock management resources – FPGA architecture – FPGA programming and resource utilization.

Unit II RTL DESIGN AND SYNTHESIS USING VERILOG HDL 9 Hours

RTL design methodology - Synthesizable Verilog HDL - Combinational and sequential RTL design - Datapath and control-path design – Parameterized RTL design - Design hierarchy and modularity - Arrays and memory modeling - Generate constructs - RTL design of arithmetic circuits – RTL synthesis - Hardware inference - FPGA resource inference - Synthesis constraints - Introduction to area, timing and power analysis.

Unit III FPGA-BASED RTL DESIGN AND OPTIMIZATION 9 Hours

FPGA resource utilization - LUT and Flip-Flop optimization - BRAM and DSP block inference – Resource sharing - Parallelism - Pipelining and retiming - Critical path analysis - Timing optimization - Area

optimization - Power-aware RTL design - Clock enable and clock gating - FSM optimization - Datapath optimization - Synthesis and implementation reports - Timing constraints.	
Unit IV SYSTEM IMPLEMENTATION	**9 Hours**
Memory-based digital system design - Single-port and dual-port RAM - Synchronous FIFO - Counter and timer design - ALU design - Digital control systems – Elevator controller - Traffic light controller - Pipelined datapath - Introduction to RISC-V processor architecture - FPGA-based processor implementation - Hardware accelerator design - FPGA-based digital system case studies.	
Unit V HARDWARE SOFTWARE CO-DESIGN	**9 Hours**
Introduction to hardware-software co-design - Hard IP and Soft IP - Processor-FPGA integration - Processing System and Programmable Logic – Memory-mapped peripheral interfacing - AXI-based communication - Hardware accelerator integration - UART-based FPGA implementation - PYNQ architecture - Python-based FPGA control - Introduction to AI model deployment on PYNQ - FPGA-based hardware acceleration - Hardware-software co-design case studies.	
Term Work Activity	
Quiz, Assignments, and Seminar Presentations.	
Self-Learning Activity	
NPTEL Course: https://nptel.ac.in/courses/108107870	
Total	**45 Hours**

References:

1. Cem Unsalan and Bora Tar, Digital System Design with FPGA: Implementation Using Verilog and VHDL, 1st Edition, McGraw-Hill Education, 2017.
2. Shirshendu Roy, Advanced Digital System Design: A Practical Guide to Verilog Based FPGA and ASIC Implementation, Springer, 2023.
3. Samir Palnitkar, Verilog HDL, Pearson Education,2ndEdition,2004.
4. Vaibbhav Taraate. Digital Logic Design Using Verilog: Coding and RTL Synthesis. 2nd Edition, Springer, 2022.
5. Ming Bo Lin, Wiley, Digital System Designs and Practices using Verilog HDL and FPGAs, 2012.
6. Bob Zeidman, Designing with FPGAs and CPLDs, Elsevier, CMP Books, 2002.

26VL14	DIGITAL INTEGRATED CIRCUIT DESIGN	L	T	P	C
		3	0	0	3

Prerequisite	Assessment Pattern		
• Knowledge of basic mathematics and algebra • Understanding of basic algorithms and problem-solving techniques	CIA	SEE	Total
	40	60	100

Course Objectives:

- Impart foundational knowledge on IC design abstraction levels, CMOS fabrication processes, and ASIC/FPGA design flows.
- Analyze the behavior of MOS transistors, explore various CMOS logic styles, and apply low-power design techniques.
- Develops competency in memory design, physical layout, and the implementation of arithmetic sub-systems in VLSI, equipping students with essential skills for advanced integrated circuit design.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Understand IC design flow and CMOS fabrication process.
2. Design MOS circuits and analyze the factors influencing the operation of CMOS transistors.
3. Analyze the speed, power, and area trade-offs of different circuit families for combinational logic and sequential logic
4. Design a semiconductor memory and the physical layout of the digital logic.
5. Design and optimize arithmetic subsystems such as adders and multipliers using VLSI techniques.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	2		2	2		
CO 2	2			3		2
CO 3	2				2	3
CO 4	3	2	3		2	
CO 5	2	2	3	3	3	2

Unit I IC DESIGN FLOW OVERVIEW AND MANUFACTURING OF CMOS INTEGRATED CIRCUITS 8 Hours

Design abstraction levels in digital circuits - Issues in Digital Integrated Circuit Design - Quality Metrics of a Digital Design - ASIC Design Flow: Full Custom and Semi-custom Approach - Silicon Semiconductor technology: Wafer Formation - Photolithography - Well and Channel Formation - Silicon Dioxide (SiO2) - Isolation - Gate Oxide - Gate and Source/Drain Formations - Contacts and Metallization - Passivation - Metrology - CMOS Fabrication.

Unit II CMOS INVERTER CHARACTERISTICS 9 Hours

MOS Operation - Second-order effect - Body effect - Channel length modulation - Subthreshold conduction - CMOS inverter: DC Characteristics - Noise Margin - Switching Characteristics - Transistor Sizing - Static & Dynamic Power Dissipation - Energy-Delay Optimization.

Unit III CMOS LOW POWER DESIGNS 11 Hours

Review of Logic Styles - CMOS Differential Logic Families - Power Dissipation in CMOS Circuits - Power Reduction Techniques: Reduction of Voltage Swing and Switching Activity - Clock Gating - Power Gating - Voltage Scaling - Multi-Voltage Design - Multi-Threshold CMOS - Dynamic Voltage and Frequency Scaling (DVFS) - Adaptive Body Biasing - Issues in Low-Power Chip Design.

Unit IV SEMICONDUCTOR MEMORIES AND PHYSICAL DESIGN 9 Hours

Conventional CMOS Latches - CMOS D Flip Flop - SDFF - TSPC Flip Flop - Memory Organization - 6T SRAM – SRAM Array - 1T DRAM – CAM Physical Design: Stick Diagrams - Layout Design Rules – Layout Design of Digital Logic.	
Unit V VLSI SUB-SYSTEM DESIGN	**8 Hours**
Carry Look-Ahead Adder – Carry Skip Adder - Carry Select Adder - Prefix Adders - Multipliers: Unsigned Array Multiplier - Two's Complement Signed Multiplier - Booth Encoding Multiplier - Low-Power Arithmetic Circuit Design - Power Distribution Networks - Clock Distribution and Clock Circuitry - Design Trade-offs in VLSI Subsystems.	
Term Work Activity	
Quiz, Assignments, and Seminar Presentations.	
Self-Learning Activity	
NPTEL Course: https://nptel.ac.in/courses/108106158	
Total	**45 Hours**
References:	
1.Neil.H.E Weste David Harris CMOS VLSI Design: A Circuits and Systems Perspective, 4th edition, Pearson Addison Wesley, 2015. 2.Rabaey, Chandrakasan and Nikolic, Digital Integrated Circuit: A design Perspective, PHI, Second Edition ,2016. 3.John P.Uyemura, Introduction to VLSI circuits and systems, John Wiley, 2016. 4.Kamran Eshraghian, Douglas A. Pucknell, Essentials of VLSI Circuits and Systems Prentice Hall of India, 2015. 5.Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata McGraw Hill, 2014 6.https://onlinecourses.nptel.ac.in/noc21_ee09/preview.	

26VL15	SEMICONDUCTOR DEVICE MODELLING	L	T	P	C
		3	0	0	3

Prerequisite	Assessment Pattern		
• Basic knowledge of semiconductor physics and electronic devices. • Fundamental understanding of diode, BJT, and MOSFET characteristics and operation. • Basic knowledge of circuit analysis and mathematical modelling techniques.	CIA	SEE	Total
	40	60	100

Course Objectives

- Understand key device performance indicators by linking process and device simulations to understand fabrication impacts on electrical characteristics.
- It highlights the role of device simulation in circuit design, strengthens analytical understanding of 1D MOSFET process and device theory, builds expertise in computer-assisted IC design techniques, and evaluates essential performance metrics for RF applications.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Understand fundamental semiconductor device analysis principles
2. Analyze PN junction characteristics using CAD simulation tools effectively.
3. Compute the threshold voltage for various general structures with process / device simulation programs.
4. Predict the physical and current-voltage properties of 3D semiconductor devices
5. Examine the important properties of a compact model for both analog and RF circuits.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	1		3			
CO 2	2	1	3	2		
CO 3	2	1	3	3		
CO 4	2		3	3		
CO 5	2		3	3	2	

Unit I FUNDAMENTALS OF SEMICONDUCTOR DEVICE 8 Hours

Introduction to semiconductor device analysis; field-effect structures; components of charge; bulk charge (QB); introduction to bipolar junction structures; bipolar device operation; equilibrium equation; non-equilibrium equation; coupled semiconductor equations; minority carrier continuity equation.

Unit II SEMICONDUCTOR DEVICE ANALYSIS USING CAD 9 Hours

Analysis of a PN junction diode using CAD tools; principles of junction operation; electric field distribution across the device for various applied voltages; potential distribution across the device for different bias conditions; PN junction carrier densities under equilibrium and non-equilibrium conditions; carrier transport and conservation principles; PN junction equilibrium conditions.

Unit III MOSFET DEVICE MODELING 9 Hours

Review of MOSFET Characteristics; MOSFET conduction band profile; energy band diagrams as functions of VDS and VGS; inversion layer functioning as a nonlinear resistor; drain current expression; threshold voltage in non-uniform substrate; computation of flat band voltage (VFB) for non-uniform doping. MOS device design by simulation; body-bias sensitivity of threshold voltage; two-region model; subthreshold characteristics; MOSFET design optimization using simulation.	
Unit IV FINFET TECHNOLOGY, SCALING AND DEVICE MODELING	**10 Hours**
FinFET structure and design considerations of threshold voltage; leakage current mechanisms; power consumption in scaled devices; high-k dielectric materials; metal gate technology; device gate engineering; process flow of FinFET simulation; FinFET 3D simulation techniques; physical property analysis of FinFET; electric-field distribution; electric potential distribution; energy band diagrams (Ec and Ev) under bias conditions.	
Unit V FINFET FOR ANALOG AND RF APPLICATIONS	**9 Hours**
Important role of FinFET in analog and RF circuits; introduction to important compact model metrics; analog performance metrics; quiescent operating point; importance of moderate region operation for analog circuits; role of leakage currents in discrete-time and low-power applications; device transconductance efficiency versus bias; device transconductance (g_m) versus VGS and VDS; Unity gain frequency and Maximum Oscillation frequency.	
Term Work Activity	
Quiz, Assignments, and Seminar Presentations.	
Self-Learning Activity	
NPTEL Course: https://nptel.ac.in/courses/117106033	
Total	**45 Hours**

References

1. Wu, Y.-C., & Jhan, Y.-R. *3D TCAD Simulation for CMOS Nanoelectronic Devices*. Springer Nature Singapore Pte Ltd., 2018.
2. Chauhan, Y. S., Lu, D. D., Sriramkumar, V., Khandelwal, S., Duarte, J. P., Payvadosi, N., Niknejad, A., & Hu, C. *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard*. Academic Press - Elsevier, 2015.
3. Armstrong, G. A., & Maiti, C. K. *TCAD for Si, SiGe and GaAs Integrated Circuits*. The Institution of Engineering and Technology, London, United Kingdom, 2007.
4. Lundstrom, M. S. *Fundamentals of Carrier Transport* (2nd ed.). Cambridge University Press, Cambridge, UK, 2000.
5. Dutton, R. W., & Yu, Z. *Technology CAD: Computer Simulation of Processes and Devices*. Kluwer Academic Publishers, 1993.
6. Synopsys Inc. *Sentaurus TCAD User Manual* (Latest Edition). Synopsys Inc.

26VL16	ANALOG INTEGRATED CIRCUIT DESIGN	L	T	P	C
		3	0	0	3

Prerequisite	Assessment Pattern		
• Fundamental knowledge of electronic devices and circuits. • Basic understanding of analog circuit analysis and semiconductor devices.	CIA	SEE	Total
	40	60	100

Course Objectives

- Design CMOS analog building blocks using device-level understanding.
- Analyze and design amplifiers and operational amplifiers.
- Evaluate frequency response, stability, and compensation techniques.
- Design circuits based on given specifications.
- Understand the basic operation of phase locked loops
- Analyze non-ideal effects in analog integrated circuits.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Analyze analog circuit building blocks using fundamental circuit-level design principles.
2. Design current mirrors, biasing circuits, and differential amplifiers for analog integrated circuit applications.
3. Evaluate single-stage and multi-stage amplifiers with frequency response analysis.
4. Develop CMOS operational amplifiers considering gain, stability, and performance requirements.
5. Understand the basic operation of phase-locked loops (PLLs) and analyze non-ideal effects in analog circuits.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	1		3	2		
CO 2	2	1	3	3	2	
CO 3	2		3	3		
CO 4	2	1	3	3	2	
CO 5	2		3	2	2	

Unit I ANALOG BUILDING BLOCKS 9 Hours

Current sources and sinks - Current mirrors (simple, cascode, Wilson) - Design equations and output resistance analysis - Differential amplifiers - Small-signal analysis - CMRR - Active loads - Gain enhancement techniques - Biasing techniques - Bandgap reference (basic principle) - Cascode structures.

Unit II AMPLIFIER DESIGN 9 Hours

Review of MOS small-signal model - Common source, common gate, source follower - Gain derivations - Output resistance - Frequency response - Poles and zeros - Dominant pole analysis - Multi-stage amplifiers - Miller compensation - Stability and phase margin.

Unit III OPERATIONAL AMPLIFIERS 9 Hours

Two-stage CMOS op-amp design - Design procedure - Telescopic and folded cascode op-amps - Gain boosting techniques - Slew rate analysis - Power dissipation - Frequency compensation techniques - Stability and phase margin - Design for specifications.

Unit IV PHASE LOCKED LOOPS 9 Hours

Basic PLL architecture - Phase detector - Charge pump - Loop filter - Voltage Controlled Oscillator (VCO) - Frequency synthesizer basics - Lock range and capture range - Applications of PLL.

Unit V	**ADVANCED ANALOG DESIGN**	**9 Hours**
Noise analysis (thermal and flicker noise) - Input-referred noise - Device mismatch - Process variations - Performance trade-offs - DAC architectures (R-2R, current steering - basics) - ADC architectures (Flash, SAR - basics) - Sample and hold circuits - Non-idealities (offset, INL, DNL).		
Term Work Activity		
Quiz, Assignments, and Seminar Presentations.		
Self-Learning Activity		
NPTEL Course: https://nptel.ac.in/courses/108106105		
	Total	**45 Hours**

References

1. Design of Analog CMOS Integrated Circuits - Behzad Razavi, McGraw-Hill Education, 2000.
2. CMOS Analog Circuit Design - Phillip E. Allen and Douglas R. Holberg, Oxford University Press, 2011 (3rd Edition).
3. Microelectronic Circuits - Adel S. Sedra and Kenneth C. Smith, Oxford University Press, 2014 (7th Edition).
4. Analysis and Design of Analog Integrated Circuits - Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, John Wiley & Sons, 2009 (5th Edition).

26VL17	DIGITAL DESIGN WITH FPGA LABORATORY	L	T	P	C
		0	0	4	2

Prerequisite	Assessment Pattern		
• Basic knowledge of Digital Electronics and Logic Circuit Design. • Basic understanding of Verilog HDL and digital circuit simulation. • Familiarity with FPGA architecture and basic computer programming concepts.	CIA	SEE	Total
	60	40	100

Course Objectives

- Develop skills in designing and implementing RTL-based digital systems using Verilog HDL on FPGA platforms.
- Provide hands-on experience in FPGA resource utilization, timing analysis, optimization, and implementation of digital subsystems.
- Develop practical skills in processor-based systems, peripheral interfacing, and hardware-software co-design using FPGA platforms such as PYNQ

Course Outcomes (COs)

At the end of the course, students will be able to

1. Design and implement synthesizable RTL-based digital circuits using Verilog HDL on FPGA platforms.
2. Implement arithmetic, sequential, memory and pipelined digital subsystems using FPGA resources.
3. Analyze and optimize FPGA implementations based on resource utilization, timing and performance.
4. Design and implement processor-based digital systems and peripheral interfaces on FPGA platforms.
5. Develop and evaluate hardware-software co-design solutions and hardware accelerators using PYNQ-based FPGA platforms.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	1		3	2		
CO 2	2	1	3	3		
CO 3	2	2	3	2		
CO 4	2		3	3		
CO 5	2	2	3	3	2	

EXPERIMENT 1 **3 Hours**

Design and FPGA Implementation of a Parameterized Arithmetic Logic Unit (ALU) Using Verilog HDL.

EXPERIMENT 2 **3 Hours**

Design and FPGA Implementation of a Configurable Up/Down Counter with Clock Enable and FSM-Based Control

EXPERIMENT 3 **4 Hours**

Design and FPGA Implementation of Single-Port RAM, Dual-Port RAM and Synchronous FIFO Using FPGA Block RAM

EXPERIMENT 4 **4 Hours**

Design and FPGA Implementation of a Pipelined Arithmetic Datapath for Improved Timing Performance

EXPERIMENT 5 **4 Hours**

Analysis and Optimization of FPGA Resource Utilization and Timing Performance Using Synthesis and Implementation Reports of Pipelined Arithmetic Data path.

EXPERIMENT 6 **4 Hours**

Design and FPGA Implementation of a RISC-V Processor-Based Digital System with Memory and Peripheral Interfaces

EXPERIMENT 7 **4 Hours**

Design and Implementation of AXI-Based Peripheral Interfacing Between Processing System and Programmable Logic

EXPERIMENT 8 **4 Hours**

Design and Implementation of a Hardware Accelerator Using PYNQ for Hardware-Software Co-Design

Total	**30 Hours**

References

1. Samir Palnitkar. Verilog HDL: A Guide to Digital Design and Synthesis (2nd ed.). Prentice Hall, 2003.
2. Brown, S., & Vranesic, Z. Fundamentals of Digital Logic with Verilog Design (3rd ed.). McGraw-Hill Education, 2014.
3. Cem Unsalan and Bora Tar, Digital System Design with FPGA: Implementation Using Verilog and VHDL, 1st Edition, McGraw-Hill Education, 2017.
4. Shirshendu Roy, Advanced Digital System Design: A Practical Guide to Verilog Based FPGA and ASIC Implementation, Springer, 2023.
5. S. Ramachandran, Digital VLSI Systems Design: A Design Manual for Implementation of Projects on FPGAs and ASICs Using Verilog, Springer, 2007.
6. Sarah L. Harris and David Harris, Digital Design and Computer Architecture: RISC-V Edition, 1st Edition, Morgan Kaufmann, 2021.

26VL18	DIGITAL AND ANALOG INTEGRATED CIRCUIT DESIGN LABORATORY	L	T	P	C
		0	0	4	2

Prerequisite	Assessment Pattern		
	CIA	SEE	Total
• Basic knowledge of Analog and Digital Electronics. • Fundamental understanding of MOSFETs, CMOS circuits, and integrated circuit design concepts. • Basic knowledge of circuit analysis, simulation tools, and electronic circuit design principles.	60	40	100

Course Objectives

- To provide hands-on experience in the design, simulation, and layout of fundamental digital and analog CMOS circuits using industry-standard EDA tools.
- To analyze the performance characteristics of digital and analog integrated circuits in terms of delay, power, noise, stability, and frequency response.
- To develop practical skills in verifying circuit functionality, understanding device-level effects, and interpreting pre- and post-layout simulation results.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Design and analyze basic CMOS digital circuits such as inverter, NAND, NOR, ring oscillator, flip-flops, and SRAM, and evaluate parameters like delay, power, and noise margins.
2. Design and evaluate analog circuits including current mirrors, differential amplifiers, and common source amplifiers with respect to gain, output resistance, and frequency response.
3. Design CMOS operational amplifiers (single-stage and two-stage) and analyze their AC and transient performance including gain, phase margin, and slew rate.
4. Perform layout design of selected digital and analog circuits and analyze the impact of parasitics through pre- and post-layout simulations.
5. Analyze non-ideal effects such as noise, mismatch, and process variations using techniques like Monte Carlo simulation and evaluate circuit robustness.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	1		3	3	2	
CO 2	1	1	3	3	3	
CO 3	2	1	3	3	3	
CO 4	2	2	3	3	3	
CO 5	2	1	3	2		

DIGITAL IC LABORATORY

EXPERIMENT 1 **3 Hours**

Design and analysis of a CMOS inverter and analyze voltage transfer characteristics (VTC), switching threshold, noise margins, propagation delay, and power dissipation. Create a layout view.

EXPERIMENT 2 **3 Hours**

Design and analysis of CMOS NAND and NOR gates and analyze logic functionality, propagation delay, power consumption, and transistor sizing effects on performance. Create a layout view.

EXPERIMENT 3 **3 Hours**

Design and analysis of a CMOS ring oscillator and analyze oscillation frequency, propagation delay per stage, power consumption, and effect of number of stages on performance.

EXPERIMENT 4 **3 Hours**

Design and analysis of a CMOS D flip-flop and analyze setup time, hold time, clock-to-Q delay, power consumption, and timing reliability.

EXPERIMENT 5 **3 Hours**

Design and analysis of a CMOS SRAM cell and analyze read/write stability, static noise margin (SNM), access time, and power consumption.

ANALOG IC LABORATORY

EXPERIMENT 1 **3 Hours**

Design and Analysis of CMOS Current Mirrors (Simple & Cascode) and analyze, Output current accuracy, Output resistance and Effect of channel length modulation.

EXPERIMENT 2 **3 Hours**

Differential Amplifier Design and CMRR Analysis of Differential gain (Ad), Common-mode gain (Ac) and CMRR.

EXPERIMENT 3 **3 Hours**

Common Source Amplifier - Gain & Frequency Response. Create a layout view.

EXPERIMENT 4 **3 Hours**

Two-Stage CMOS Op-Amp Design and Performance of AC analysis (gain, phase margin) and Transient (slew rate). Create a Layout view.

EXPERIMENT 5 **3 Hours**

Noise and Mismatch Analysis in CS amplifier / differential amplifier circuits, Input-referred noise and perform Monte-Carlo simulation for mismatch.

Total	**30 Hours**

References

1. Razavi, B. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education, 2000.
2. Allen, P. E., & Holberg, D. R. *CMOS Analog Circuit Design* (3rd ed.). Oxford University Press, 2011.
3. Sedra, A. S., & Smith, K. C. *Microelectronic Circuits* (7th ed.). Oxford University Press, 2014.
4. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. *Analysis and Design of Analog Integrated Circuits* (5th ed.). John Wiley & Sons, 2009.
5. Kang, S. M., & Leblebici, Y. *CMOS Digital Integrated Circuits: Analysis and Design* (4th ed.). McGraw-Hill Education, 2015.
6. Baker, R. J. *CMOS: Circuit Design, Layout, and Simulation* (3rd ed.). Wiley-IEEE Press, 2010.
7. Weste, N. H. E., & Harris, D. *CMOS VLSI Design: A Circuits and Systems Perspective* (4th ed.). Pearson Education, 2011.
8. Johns, D., & Martin, K. *Analog Integrated Circuit Design*. Wiley India Pvt. Ltd., 2008.

26VL21	VLSI SCRIPTING LANGUAGES	L	T	P	C
		3	0	0	3

Prerequisite	Assessment Pattern		
• Fundamentals of VLSI design and digital electronics. • Basic knowledge of Python/TCL programming and scripting concepts.	CIA	SEE	Total
	40	60	100

Course Objectives:

- To illustrate the various scripting languages in VLSI.
- To interpret the basic of Linux, TCL fundamentals and Python scripting.
- To learn the applications of linux, Python, TCL and Advanced TCL scripting.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Understand Fundamental knowledge of the Linux operating system and its command-line environment.
2. Introduce scripting languages and their significance in EDA workflows, along with the differences between scripting and compiled languages.
3. Enable the use of Python scripting for automation and application development in VLSI design.
4. Develop proficiency in TCL scripting for controlling and automating EDA tool operations.
5. Design advanced TCL-based automation scripts for managing and optimizing VLSI design processes.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	1	1	3	1	1	
CO 2	2	2	3	2	1	
CO 3	2	2	3	3	2	
CO 4	2	2	3	3	3	
CO 5	3	3	3	3	3	

Unit I LINUX CONCEPTS 8 Hours

Introduction to Linux, File System of the Linux, General usage of Linux kernel 7 basic commands, Linux users and group, Permissions for file, directory and users, Searching a file & directory, Zipping and unzipping concepts, Shell Scripting.

Unit II INTRODUCTION TO SCRIPTING LANGUAGES IN EDA 8 Hours

Introduction to scripting and automation, Scripting vs compiled languages, using interpreters and writing first scripts in Perl, Tcl, and Python, Command-line execution, Variable types and assignments (overview), Control flow basics (if, loops - overview), Basic file I/O (overview), Importance of scripting in EDA tools and flows.

Unit III PYTHON SCRIPTING 9 Hours

Introduction to Python, Program Development Cycle, Data types and Expressions, more about Data Output, Performing Calculations, Loops and lists, Data Structures, Modules, Input and Output, Errors and Exceptions, Classes, Functions and Modules, Floating Point Arithmetic, Tour of the Standard Python Libraries.

Unit IV TCL SCRIPTING 10 Hours

Tcl syntax and structure, Variables and data types, Lists and arrays, Expressions and operators, Control flow (if, switch, while, for, for each), Procedures and variable scope, File input and output, String and list manipulation, Error handling, Working with commands and arguments, Tool-specific scripting conventions, Example tool scripts for synthesis and simulation.

Unit V ADVANCED SCRIPTING 10 Hours

Advance TCL- eval, source, exec and up level commands, Name spaces, trapping errors, event driven programs, making applications internet aware, Nuts and Bolts Internet Programming, Security Issues, C Interface. Tk- Visual Tool Kits, Fundamental Concepts of Tk, Tk by example, Events and Binding, Perl-Tk.	
Term Work Activity	
Quiz, Assignments, and Seminar Presentations.	
Self-Learning Activity	
NPTEL Course	
Total	**45 Hours**

References:

1. Barron, D. *The World of Scripting Languages*. Wiley Publications, 2000.
2. Holden, S., & Beazley, D. *Python Web Programming*. New Riders Publications, 2002.
3. Naik, G. S. *Learning Linux Shell Scripting*. Packt Publishing Ltd., 2015.
4. Van Rossum, G., & Drake Jr., F. L. *An Introduction to Python* (2nd ed.). Network Theory Ltd., 2011.
5. Langtangen, H. P. *A Primer on Scientific Programming with Python* (5th ed.). Springer, 2016.
6. Welch, B. B., Jones, K., & Hobbs, J. *Practical Programming in Tcl and Tk* (4th ed.). Prentice Hall, 2003.
7. Sweigart, A. *Automate the Boring Stuff with Python: Practical Programming for Total Beginners* (2nd ed.). No Starch Press, 2019.
8. Ousterhout, J. K. *Tcl and the Tk Toolkit* (2nd ed.). Addison-Wesley Professional, 2009.

26VL22	SYSTEM VERILOG FOR VERIFICATION	L	T	P	C
		3	0	0	3

Prerequisite	Assessment Pattern		
• Fundamentals of digital electronics, VLSI design, and RTL design. • Basic knowledge of Verilog/HDL programming and computer architecture.	CIA	SEE	Total
	40	60	100

Course Objectives:

- Develop an understanding of SystemVerilog language constructs and programming concepts.
- Introduce System Verilog features for unified design, testing, and verification.
- Provide knowledge of SystemVerilog-based testing, verification, and functional coverage techniques.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Apply System Verilog language constructs, data types, arrays, and testbench methodologies for digital design verification.
2. Develop procedural blocks, tasks, functions, structures, and enumerated data types for verification-oriented programming.
3. Design object-oriented verification environments using classes, objects, methods, and layered testbench architectures.
4. Implement constrained random verification techniques and coverage-driven verification methodologies using SystemVerilog.
5. Analyze and measure functional coverage, cross coverage, and assertion-based verification metrics for validating digital systems.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	1	1	3	2	1	
CO 2	2	2	3	3	1	
CO 3	2	2	3	3	2	
CO 4	3	2	3	3	2	
CO 5	3	3	3	3	3	1

Unit I VERIFICATION GUIDELINES & DATA TYPES 9 Hours

The Verification Process, Basic Test Bench Functionality, Directed testing, Methodology Basics, Logic & 2 state Data Types, typedef, enum, struct, package, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Array Methods.

Unit II INTERFACE AND SUBROUTINES 9 Hours

Interface, modports, Clocking block, Task and Function Overview, Tasks, Functions, and Void Functions, subroutine Arguments, returning from a subroutine, Pass by reference, Automatic Taks/Functions.

Unit III OOPs 9 Hours

Classes and Objects, Class Declaration, Creating Objects, Constructors, Object Handles, Object Deallocation, Class Properties and Methods, Methods Inside and Outside the Class, Static Variables and Static Methods, Scope Resolution, Nested Classes, Object Copying, Shallow Copy and Deep Copy, Encapsulation, Inheritance, Method Overriding, Polymorphism, Virtual Methods, Abstract Classes, Parameterized Classes, OOP-Based Testbench.

Unit IV	**RANDOMIZATION**	**9 Hours**
Randomization in System Verilog, rand & ranc constructs, constraints in randomization, controlling multiple constraint blocks, set membership, in-line constraints, pre-randomize and post randomize, Atomic and scenario generation, Revisiting the code coverage and functional coverage with randomization.		
Unit V	**FUNCTIONAL COVERAGE**	**9 Hours**
Gathering Coverage Data, Coverage Types, Functional Coverage Strategies, built-in methods of covergroup, Simple functional Coverage examples, Anatomy of a cover group, triggering a cover group. Data Sampling, Cross coverage, Generic cover groups, Coverage Options, Analyzing Coverage Data, and Measuring Coverage Statistics during simulation, System Verilog Assertions.		
Term Work Activity		
Quiz, Assignments, and Seminar Presentations.		
Self-Learning Activity		
NPTEL Course: https://nptel.ac.in/courses/108103179		
	Total	**45 Hours**

References:

1. Spear, C. SystemVerilog for Verification: A Guide to Learning the Testbench Language
2. Features (3rd ed.). Springer-Verlag New York, Inc., 2012. ISBN: 978-1-4614-0714-0.
3. Mintz, M., & Ekendahl, R. Hardware Verification with SystemVerilog: An Object-
4. Oriented Framework. Springer, USA, 2007. ISBN: 0-387-71738-2.
5. Sutherland, S., Davidmann, S., & Flake, P. SystemVerilog for Design: A Guide to Using
6. SystemVerilog for Hardware Design and Modeling. Springer, USA, 2013. ISBN:
7. 9781475766820, 1475766823.
8. ChipVerify SystemVerilog Tutorial: https://chipverify.com/systemverilog/
9. VLSI Verify SystemVerilog Tutorial: https://vlsiverify.com/systemverilog/

26VL23	VLSI PHYSICAL DESIGN	L	T	P	C
		3	0	0	3

Prerequisite	Assessment Pattern		
• Fundamentals of digital electronics, VLSI design, and CMOS technology. • Basic knowledge of Verilog/HDL, RTL design, and computer architecture.	CIA	SEE	Total
	40	60	100

Course Objectives:

- Understand the VLSI physical design flow and ASIC implementation methodologies.
- Learn floor planning, partitioning, placement, routing, timing, power, and congestion analysis.
- Understand physical verification techniques, including DRC, LVS, parasitic extraction, signal integrity, and design closure.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Understand the VLSI physical design flow, design methodologies, and technology constraints used in ASIC implementation.
2. Perform floor planning, partitioning, power planning, and placement of digital circuits using optimization techniques.
3. Apply routing algorithms, clock tree synthesis, and congestion management techniques in VLSI physical design.
4. Analyze timing, power dissipation, and signal integrity issues using timing and power optimization methods.
5. Perform physical verification, parasitic extraction, and design closure to achieve successful tape-out of VLSI circuits.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	1	1	3	2	1	
CO 2	2	2	3	3	2	
CO 3	2	2	3	3	2	
CO 4	3	2	3	3	2	2
CO 5	3	3	3	3	3	1

Unit I INTRODUCTION TO PHYSICAL DESIGN 9 Hours

Overview of VLSI Design Flow_ Full Custom, Semi-Custom and ASIC Design_ Physical Design Steps: Partitioning, Floor planning, Placement, Routing-Design Constraints and Technology Libraries- Introduction to EDA Tools.

Unit II FLOOR PLANNING AND PLACEMENT 9 Hours

Floor planning Concepts and Objectives-Partitioning Techniques-Power Planning and I/O Placement-Algorithms: Min-cut, Analytical, Force-directed- Congestion Analysis and Optimization.

Unit III ROUTING TECHNIQUES 9 Hours

Routing Fundamentals-Global Routing and Detailed Routing-Routing Algorithms: Maze Routing, Line Search-Clock Tree Synthesis (CTS)-Crosstalk and Signal Integrity Issues.

Unit IV TIMING AND POWER ANALYSIS 9 Hours

Static Timing Analysis (STA)-Setup and Hold Violations-Timing Optimization Techniques-Power Dissipation: Dynamic and Static Power-Power Reduction Techniques.

Unit V PHYSICAL VERIFICATION AND DESIGN CLOSURE	**9 Hours**
Design Rule Check (DRC)-Layout Versus Schematic (LVS)-Parasitic Extraction-Electro migration and IR Drop Analysis-Design Closure and Tape-out Process.	
Term Work Activity	
Quiz, Assignments, and Seminar Presentations.	
Self-Learning Activity	
NPTEL Course: https://nptel.ac.in/courses/108107380	
Total	**45 Hours**

References:

1. Sarrafzadeh, M., & Wong, C. K. An Introduction to VLSI Physical Design. McGraw-Hill International Edition, New York, 1996.
2. Preas, B. T., & Lorenzetti, M. J. Physical Design Automation of VLSI Systems. Benjamin/Cummings Publishing Company, 1988.
3. Kahng, A. B., Lienig, J., Markov, I. L., & Hu, J. VLSI Physical Design: From Graph Partitioning to Timing Closure. Springer, Netherlands, 2011.
4. Sherwani, N. A. Algorithms for VLSI Physical Design Automation (3rd ed.). Springer Science & Business Media, 1999.
5. Lim, S. K. Practical Problems in VLSI Physical Design Automation. Springer, USA, 2008.
6. Cadence. Cadence Physical Design Tool Documentation. Cadence Design Systems, Latest Edition.
7. Synopsys. Synopsys IC Compiler and Physical Design Documentation. Synopsys Inc., Latest Edition.
8. Siemens EDA (formerly Mentor Graphics). Mentor Graphics Physical Design Tool Documentation. Siemens EDA, Latest Edition.

26VL24	DESIGN FOR TESTABILITY (DFT)	L	T	P	C
		3	0	0	3

Prerequisite	Assessment Pattern		
• Fundamentals of digital electronics, VLSI design, and CMOS technology. • Basic knowledge of Verilog/HDL, RTL design, and digital circuit testing.	CIA	SEE	Total
	40	60	100

Course Objectives:

- Understand VLSI testing concepts, fault models, fault equivalence, and fault dominance in digital circuits.
- Learn fault simulation and Automatic Test Pattern Generation (ATPG) techniques to improve fault coverage.
- Explore Design for Testability (DFT) methodologies, including scan-based testing, BIST, boundary scan, and test compression techniques.

Course Outcomes (COs)

At the end of the course, students will be able to

1. Understand fault models, fault simulation techniques, and testing challenges in VLSI circuits.
2. Apply ATPG algorithms and testability analysis techniques for combinational circuit testing.
3. Design scan-based DFT architectures and implement scan design methodologies for digital systems.
4. Analyze and implement Built-In Self-Test (BIST) architectures and pseudo-random testing techniques.
5. Apply boundary scan standards, test compression, and response compaction techniques for core-based VLSI testing.

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	2	1	3	2	1	
CO 2	3	2	3	3	2	
CO 3	2	2	3	3	3	
CO 4	3	2	3	3	2	
CO 5	3	3	3	3	3	1

Unit I FAULT MODELLING 9 Hours

Importance of Testing - Testing during the VLSI Lifecycle - Challenges in the VLSI Testing: Test Generation - Fault Models - Levels of Abstraction in VLSI Testing - Historical Review of VLSI Test Technology - Functional Versus Structural Testing - Levels of Fault Models - Fault Equivalence - Fault Dominance - Fault Collapsing - Check point Theorem - Delay Fault.

Unit II FAULT SIMULATION AND TEST GENERATION 9 Hours

Fault Simulation: Serial, Parallel, Deductive, Concurrent - Combinational Test Generations - ATPG for Combinational Circuits - D-Algorithm - Testability Analysis - SCOAP measures for Combinational Circuits.

Unit III SCAN BASED TESTING 9 Hours

Design for Testability Basics - Ad Hoc Approach - Structured Approach - Scan Cell Designs - Scan Architectures - Scan Design Rules - Scan Design Flow - Special Purpose Scan Designs - RTL Design for Testability.

Unit IV BUILT-IN SELF-TEST 9 Hours

BIST Design Rules - Test Pattern Generation - Exhaustive Testing - Pseudo-Random Testing - Pseudo-Exhaustive Testing - Delay Fault Testing - Output Response Analysis - Logic BIST Architectures - BIST Architectures for Circuits with and without Scan Chains.

Unit V	**BOUNDARY SCAN AND CORE BASED TESTING**	**9 Hours**
Digital Boundary Scan (IEEE Std. 1149.1): Test Architecture and Operations - On-Chip Test Support with Boundary Scan - Board and System-Level Boundary-Scan Control Architectures. Test Stimulus Compression: Code-Based Schemes, Linear-Decompression-Based Schemes - Test Response Compaction.		
Term Work Activity		
Quiz, Assignments, and Seminar Presentations.		
Self-Learning Activity		
NPTEL Course: https://nptel.ac.in/courses/117105137		
	Total	**45 Hours**

References:

1. Navabi, Z. Digital System Test and Testable Design. Springer, 2011.
2. Wang, L.-T., Wu, C.-W., & Wen, X. VLSI Test Principles and Architectures. Morgan Kaufmann Publishers, 2013.
3. Bushnell, M. L., & Agrawal, V. D. Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits. Kluwer Academic Publishers, 2017.
4. Jha, N. K., & Gupta, S. Testing of Digital Systems. Cambridge University Press, 2017.
5. Lala, P. K. Digital Circuit Testing and Testability. Academic Press, 1997.
6. Abramovici, M., Breuer, M. A., & Friedman, A. D. Digital Systems Testing and Testable Design. IEEE Press, 1990.

26VL27	**RTL to GDSII Laboratory**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**

Prerequisite	**Assessment Pattern**		
• Basic knowledge of Digital Electronics and Logic Design. • Basic understanding of Verilog HDL and digital system design. • Familiarity with computer architecture and VLSI design concepts.	CIA	SEE	Total
	60	40	100

Course Objectives:

- Understand the complete ASIC design flow from RTL design to GDSII generation using industry-standard EDA tools.
- Develop Verilog HDL-based digital designs such as ALU, Counter, Memory, UART, FIFO, and RISC-V CPU architectures.
- Perform synthesis, floorplanning, placement, routing, and timing verification for VLSI digital systems.
- Analyze and compare pre-synthesis and post-synthesis parameters including area, power, and delay

Course Outcomes (COs)

At the end of the course, students will be able to

1. Apply knowledge of digital design to code Verilog modules and perform compilation, elaboration, and simulation.
2. Analyze and synthesize RTL designs into optimized gate-level implementations considering constraints
3. Evaluate design correctness using DFT techniques and equivalence checking across multiple design stages.
4. Develop physical layouts using floor planning, placement, CTS, and routing techniques.
5. Ensure design reliability through signoff checks and generate GDSII for fabrication readiness.

Articulation Matrix

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO 1	1	1	3	2	1	
CO 2	2	2	3	3	2	
CO 3	3	2	3	3	2	
CO 4	2	2	3	3	3	
CO 5	3	3	3	3	3	1

EXPERIMENT 1 **6 Hours**

Design an ALU in Verilog and implement complete RTL to GDSII flow

Generate and analyze pre-synthesis (RTL) and post-synthesis reports for area, power, and delay using automated scripts

EXPERIMENT 2 **6 Hours**

Design a counter and execute full ASIC flow.

Automate extraction and comparison of area, timing, and power reports before and after synthesis.

EXPERIMENT 3 **6 Hours**

Design memory (SRAM/ROM) and implement full flow.

Perform pre- and post-synthesis analysis and script-based report generation

EXPERIMENT 4 **6 Hours**

Design UART module and execute complete flow. Develop scripts to automate report extraction and performance comparison	
EXPERIMENT 5	**6 Hours**
Design FIFO and carry through complete ASIC flow. Analyze timing, area utilization, and power consumption across design stages using scripts	
EXPERIMENT 6	**6 Hours**
Design a basic single cycle RISC-VCPU architecture and execute full RTL to GDSII flow. Perform detailed pre- and post-synthesis performance evaluation using automated scripting.	
Total	**30 Hours**

References:

1. Weste, N. H. E., & Harris, D. *CMOS VLSI Design: A Circuits and Systems Perspective* (4th ed.). Pearson Education, 2011.
2. Sherwani, N. A. *Algorithms for VLSI Physical Design Automation* (3rd ed.). Springer Science & Business Media, 1999.
3. Kahng, A. B., Lienig, J., Markov, I. L., & Hu, J. *VLSI Physical Design: From Graph Partitioning to Timing Closure*. Springer, 2011.
4. Kang, S. M., & Leblebici, Y. *CMOS Digital Integrated Circuits: Analysis and Design* (4th ed.). McGraw-Hill Education, 2015.
5. Bhasker, J. *A Verilog HDL Primer* (3rd ed.). Star Galaxy Publishing, 2004.
6. Palnitkar, S. *Verilog HDL: A Guide to Digital Design and Synthesis* (2nd ed.). Prentice Hall, 2003.
7. Navabi, Z. *Digital System Test and Testable Design*. Springer, 2011.
8. Patterson, D. A., & Hennessy, J. L. *Computer Organization and Design: RISC-V Edition*. Morgan Kaufmann, 2020.

26VL28	DESIGN VERIFICATION LABORATORY	L	T	P	C
		0	0	4	2

Prerequisite	Assessment Pattern		
• Digital Logic Design • Verilog HDL Programming • Basic VLSI Concepts • Digital System Design	CIA	SEE	Total
	60	40	100

Course Objectives:

- Develop expertise in System Verilog-based verification methodologies.
- Design self-checking, reusable testbenches.
- Apply constrained random verification, assertions, and coverage.
- Verify digital designs ranging from simple combinational to protocol-based systems.
- Introduce industry-oriented verification practices

Course Outcomes (COs)

At the end of the course, students will be able to

1. Develop System Verilog-based testbenches for digital designs.
2. Apply constrained-random verification techniques and stimulus generation
3. Implement self-checking mechanisms using scoreboards and reference models.
4. Use assertions and functional coverage for design validation.
5. Verify complex designs including FSMs, memories, CDC, and communication protocols

Articulation Matrix

COs	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	1	2	3	2	1	
CO 2	2	2	3	3	2	
CO 3	3	2	3	3	2	
CO 4	3	2	3	3	2	
CO 5	3	3	3	3	3	

EXPERIMENT 1 - PARITY GENERATOR AND CHECKER VERIFICATION **4 Hours**

Verify the parity generator and checker using randomized input patterns and fault injection techniques. Use assertions to validate correctness and generate functional and fault coverage reports to analyze detection efficiency and completeness

EXPERIMENT 2 - ALU VERIFICATION **4 Hours**

Verify the functional correctness of the ALU using constrained-random inputs covering all arithmetic and logical operations. Implement a reference model for self-checking and generate functional and code coverage reports to ensure complete operation validation.

EXPERIMENT 3- ELEVATOR CONTROLLER VERFICATION **4 Hours**

Verify the FSM-based elevator controller for correct state transitions, request handling, and direction control using constrained stimulus. Use assertions to detect illegal states and generate functional coverage reports to ensure complete state and transition cove.

EXPERIMENT 4 - MEMORY VERIFICATION **5 Hours**

Verify memory functionality using randomized read and write operations across all address locations with a scoreboard mechanism. Use assertions for protocol checking and generate functional and code coverage reports to validate complete memory operation.

EXPERIMENT 5 - ASYNCHRONOUS FIFO VERIFICATION **4 Hours**

Verify data transfer across different clock domains in an asynchronous FIFO using independent read and write clocks. Use assertions to detect overflow and underflow conditions and generate functional coverage reports to validate corner-case scenarios.

EXPERIMENT 6 - APB CONTROLLER VERIFICATION **4 Hours**

Verify APB protocol compliance for read and write transactions using a self-checking testbench. Use assertions to validate protocol timing and generate functional and protocol coverage reports to ensure complete transaction verification.

EXPERIMENT 7 - UART VERIFICATION **5 Hours**

Verify UART transmission and reception for correct serial communication, including start/stop bits and baud rate handling. Use assertions to ensure protocol correctness and generate functional and error coverage reports to validate all communication scenarios.

Term Work Activity	
Quiz, Assignments, and Seminar Presentations.	
Self-Learning Activity	
NPTEL Course	
Total	**30 Hours**

References:

1. Weste, N. H. E., & Harris, D. *CMOS VLSI Design: A Circuits and Systems Perspective* (4th ed.). Pearson Education, 2011.
2. Sherwani, N. A. *Algorithms for VLSI Physical Design Automation* (3rd ed.). Springer Science & Business Media, 1999.
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